IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)

Sponsor

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Abstract: This standard, in conjunction with IEEE Std 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family, defines the physical and environmental layers of a PCI mezzanine card (PMC) family to be usable on (but not limited to) single slot VME, VME64 and VME64x boards, CompactPCI boards, Multibus I and Multibus II boards, desktop computers, portable computers, servers, and similar types of applications. The electrical and logical layers are based on the PCI specification from the PCI Special Interest Group. The PCI mezzanine cards allow for a variety of optional function expansions for the host system. I/O functionality from the PMC may be either through the mezzanine front panel, or via the backplane by routing the I/O signals through the mezzanine connector to the host.
Keywords: backplane I/O, bezel, board, card, CompactPCI, face plate, front panel I/O, metric, host computer, I/O, local bus, mezzanine, module, modular I/O, PCI, Multibus I, Multibus II, VME, VME64, VME64x, VMEbus

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Introduction

[This introduction is not part of IEEE Std 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC).]

This standard provides the specifications for implementing the PCI local bus between a host and mezzanine card, based on IEEE Std 1386-2001, for usage on VME64x boards, CompactPCI boards, and Multibus I and Multibus II boards. PCI boards defined for the general personal computer market will not fit on these boards since they mount perpendicular on the host computer. This standard provides the necessary mechanical and environmental requirements for the use of PCI-based mezzanine cards in a large variety of low-profile applications. PCI mezzanine cards can provide front bezel I/O, backplane I/O via the host, additional local host functions, or a combination of the three.

Special thanks are due to Dave Moore, original P1386.1 Working Group Draft Editor, for the generation of the many drafts, and Rick Spratt, Cliff Lupien, Harry Parkinson, Chau Pham and Heinz Horstmeier for their contribution to development of this standard.

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IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)

1. Overview

1.1 Scope

This standard defines a family of slim modular mezzanine cards for VME, VME64 and VME64x boards, CompactPCI® boards, Multibus® I and II boards, desktop computers, portable computers, servers, and other computer systems with the logical and electrical layers based on the Peripheral Component Interface (PCI) specification from the PCI Special Interest Group.

The complete physical (mechanical) and environmental layers are specified within IEEE Std 1386-2001.[1]

1.2 Purpose

PCI is a high-speed local bus being used by a variety of microprocessors. The PCI specification defines multiple board sizes that plug into computer mother boards in a perpendicular fashion. These perpendicular boards are not usable for low-profile computer applications. This standard defines the mechanics of a slim, modular, parallel mezzanine card family that uses the logical and electrical layers of the PCI specification for the local bus. I/O can be via the front bezel and/or through the connector to the host computer for backplane I/O. Additional local functionality also can be provided by these mezzanine cards.

1.3 General arrangement

PCI mezzanine cards (PMC) are intended to be used where slim, parallel board mounting is required such as in single board computer host modules with the addition of expander cards or option cards, as illustrated in Figure 1. The PMC may be mounted with instruments and panels that comply with the requirements of IEEE Std 1386-2001.

For maximum utilization of component space, the mezzanine card is typically placed such that the major component side of the mezzanine card faces the major component side of the host board.

[1]Information on references can be found in Clause 2.

1.4 Dimensions

All mechanical dimensions are specified in 1386-2001. All dimensions are in millimeters (mm).

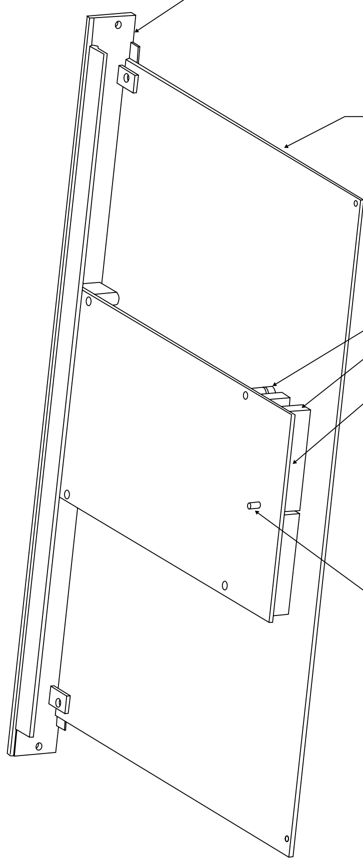

Figure 1—Typical PMC mounted to a host module

2. References

The following publications are used in conjunction with this standard. When any of the referenced specifications are superseded by an approved revision, that revision shall apply.

IEEE Std 1386-2001, IEEE Standard Mechanics for a Common Mezzanine Card (CMC) Family[2]

PCI Local Bus Specification, Revision 2.2, 1998[3]

[2]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://standards.ieee.org/).

[3]PCI specifications are available from PCI Special Interest Group (http://www.pcisig.com/).

3. Definitions

3.1 Special word usage

3.1.1 shall: A keyword indicating a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeably and to claim conformance with the specification. The phrase *is required* is used interchangeably with the keyword *shall*.

3.1.2 should: A keyword indicating flexibility of choice with a strongly preferred implementation. The phrase *is recommended* and the word *preferred* are used interchangeably with the keyword *should*.

3.1.3 may: A keyword indicating flexibility of choice with no implied preference. The phrase *is optional* is used interchangeably with the keyword *may.*

4. Mechanics and compliance

4.1 Conformance

A vendor of host modules or mezzanine cards may claim compliance to this standard if there are no areas of conflict between the host design and IEEE Std 1386-2001 or this standard. In addition, the vendor claiming compliance shall specify in the product specifications those areas of compliance where optional features are allowed.

4.2 PMC voltage keying

The PCI bus uses either 3.3 V or 5 V for signaling bus levels. A voltage keying is required to prevent association of host slots and mezzanine card with incompatible signaling voltages. The host shall indicate in its product specification which signaling voltage it uses and has been keyed for. Note that the mezzanine card may be designed to accept either or both signaling voltages.

For keying mechanics, see IEEE Std 1386-2001.

4.3 Connector configurations

The 32-bit PCI bus requires two 64-pin connectors, Pn1/Jn1 and Pn2/Jn2. The 64-bit PCI bus requires three 64-pin connectors, Pn1/Jn1, Pn2/Jn2 and Pn3/Jn3. When I/O is routed through the host's backplane, the Pn4/Jn4 connector is required for routing of the I/O signals. Any combination of the three connector functions may be used on the mezzanine card as well as on the host.

4.4 Power consumption, heat dissipation, and air flow

Each PMC vendor shall document in the product's information the current drawn on the 5 V and 3.3 V power pins. The average heat dissipated on both sides shall be given, as well as the average percent of area (side view) occupied by the components. A user can then calculate the amount of air flow that can be expected to flow across each mezzanine card as well as the amount of air needed to properly cool the mezzanine card.

4.5 Electromagnetic compatibility

Each PMC vendor shall document in the product's literature to which electromagnetic compatibility (EMC) standards and to what level(s) the product was designed and tested to (if tests were performed).

4.6 Shock and vibration

Each PMC vendor shall document in the product's literature to which shock and vibration standards and to what level(s) the product was designed and tested to (if tests were performed).

4.7 Environmental

Each PMC vendor shall document in the product's literature to which environmental standards and to what level(s) the product was designed and tested (if tests were performed).

4.8 Mean-time-between-failure (MTBF)

Each PMC vendor shall state in the product's literature the calculated mean-time-between-failure (MTBF) for which environmental level, and state what method was used to calculate the MTBF number(s).

5. Electrical and logical layer

5.1 Connector utilization

The PMC and associated host connector pin assignments are based on specific signal integrity rules as well as power distribution. The 5 V pins are assigned to Pn1/Jn1 connector, the 3.3 V pins are assigned to Pn2/Jn2 connector, and the V(I/O) to Pn1/Jn1 and Pn3/Jn3 connectors. All signal pins are adjacent to a voltage or ground pin with the clock (CLK) pin surrounded by three ground pins.

The Pn1/Jn1 and Pn2/Jn2 connectors are always present and contain the signals for the 32-bit PCI Bus. When the PCI Bus is expanded to 64 bits, the Pn3/Jn3 connector is used for these signals. User defined I/O signals are assigned to the Pn4/Jn4 connector. The Pn3/Jn3 and Pn4/Jn4 connectors do not need to be present on either the PCI mezzanine card (PMC) or the host when those signals are not used. Use of PCI bus reserve (PCI-RSVD) and PMC reserved (PMC-RSVD) pins are not allowed as their use may be defined by future versions of the PCI specifications or by this standard, respectively. All Pn1/Jn1 and Pn2/Jn2 connector pins are fixed and shall not be reassigned to other functions.

Note that the PCI signals are completely defined in PCI Local Bus Specification, Revision 2.2, 1998.

Pn4/Jn4 connectors are for user-defined I/O functions. The mapping of these I/O signals to the backplane is defined in IEEE Std 1386-2001 for Multibus applications. Mapping of I/O signals off the rear of VME boards through VME backplanes is defined and controlled by the VME International Trade Association (VITA).[4] Mapping of I/O signals off the rear of CompactPCI boards through CompactPCI backplanes is defined and controlled by the PCI Industrial Computer Manufacturers Group (PICMG®).[5]

5.2 PMC connector pin assignment

PCI mezzanine cards and associated hosts that support PMC slots shall assign the local bus signal pins per the pin assignment given in Table 1.

See Figure 2 and Figure 3 for connector orientation on the PMC and on the associated host, respectively.

[4]Information on VITA is available on the World Wide Web at the following URL: http://www.vita.com.
[5]Information on PICMG is available on the World Wide Web at the following URL: http://www.picmg.com.

Table 1—PMC connector pin assignments

Pn1/Jn1 32-bit PCI			
Pin	Signal	Signal	Pin
1	TCK	–12 V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5 V	8
9	INTD#	PCI-RSVD*	10
11	Ground	3.3 Vaux	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5 V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5 V	30
31	V (I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5 V	38
39	Ground	LOCK#	40
41	PCI-RSVD*	PCI-RSVD*	42
43	PAR	Ground	44
45	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5 V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5 V	62
63	Ground	REQ64#	64

Pn2/Jn2 32-bit PCI			
Pin	Signal	Signal	Pin
1	+12 V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	BUSMODE2#	+3.3 V	12
13	RST#	BUSMODE3#	14
15	3.3 V	BUSMODE4#	16
17	PME#	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3 V	24
25	IDSEL	AD[23]	26
27	+3.3 V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3 V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3 V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3 V	50
51	AD[07]	PMC-RSVD	52
53	+3.3 V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3 V	62
63	Ground	PMC-RSVD	64

Pn3/Jn3 64-bit PCI			
Pin	Signal	Signal	Pin
1	PCI-RSVD	Ground	2
3	Ground	C/BE[7]#	4
5	C/BE[6]#	C/BE[5]#	6
7	C/BE[4]#	Ground	8
9	V (I/O)	PAR64	10
11	AD[63]	AD[62]	12
13	AD[61]	Ground	14
15	Ground	AD[60]	16
17	AD[59]	AD[58]	18
19	AD[57]	Ground	20
21	V (I/O)	AD[56]	22
23	AD[55]	AD[54]	24
25	AD[53]	Ground	26
27	Ground	AD[52]	28
29	AD[51]	AD[50]	30
31	AD[49]	Ground	32
33	Ground	AD[48]	34
35	AD[47]	AD[46]	36
37	AD[45]	Ground	38
39	V (I/O)	AD[44]	40
41	AD[43]	AD[42]	42
43	AD[41]	Ground	44
45	Ground	AD[40]	46
47	AD[39]	AD[38]	48
49	AD[37]	Ground	50
51	Ground	AD[36]	52
53	AD[35]	AD[34]	54
55	AD[33]	Ground	56
57	V (I/O)	AD[32]	58
59	PCI-RSVD	PCI-RSVD	60
61	PCI-RSVD	Ground	62
63	Ground	PCI-RSVD	64

Pn4/Jn4 user-defined I/O			
Pin	Signal	Signal	Pin
1	I/O	I/O	2
3	I/O	I/O	4
5	I/O	I/O	6
7	I/O	I/O	8
9	I/O	I/O	10
11	I/O	I/O	12
13	I/O	I/O	14
15	I/O	I/O	16
17	I/O	I/O	18
19	I/O	I/O	20
21	I/O	I/O	22
23	I/O	I/O	24
25	I/O	I/O	26
27	I/O	I/O	28
29	I/O	I/O	30
31	I/O	I/O	32
33	I/O	I/O	34
35	I/O	I/O	36
37	I/O	I/O	38
39	I/O	I/O	40
41	I/O	I/O	42
43	I/O	I/O	44
45	I/O	I/O	46
47	I/O	I/O	48
49	I/O	I/O	50
51	I/O	I/O	52
53	I/O	I/O	54
55	I/O	I/O	56
57	I/O	I/O	58
59	I/O	I/O	60
61	I/O	I/O	62
63	I/O	I/O	64

*For PCI-RSVD/PMC pin relationship, see Table 3.

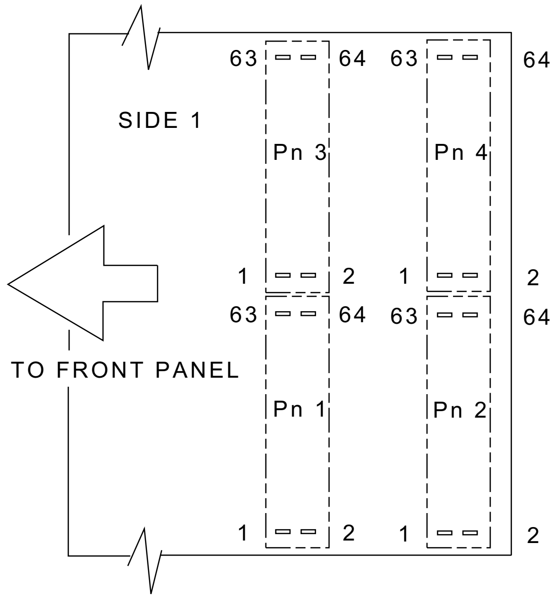

Figure 2—Connector orientation on PMC, side 1

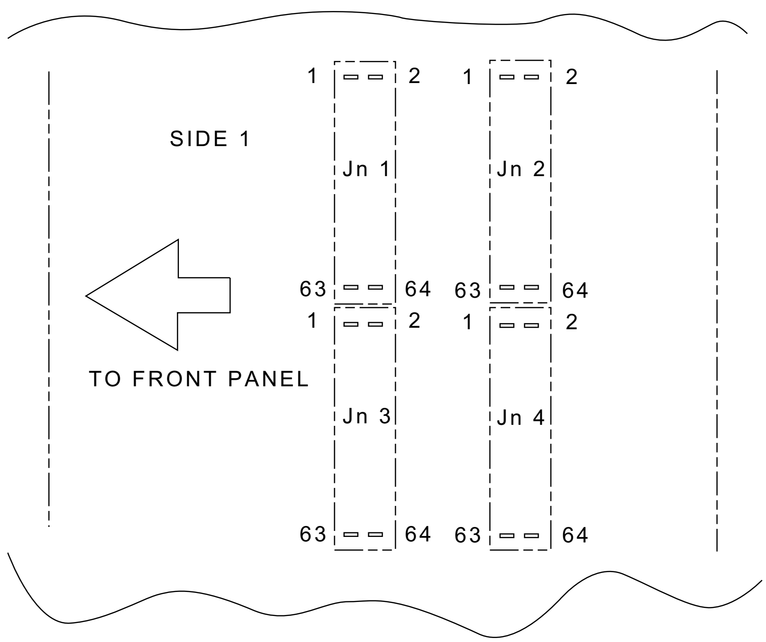

Figure 3—Connector orientation on host, side 1

5.3 Comparison of pin usage, PCI to PMC

For reference purposes, a comparison of pin usage, PCI to PMC, is provided in Table 2, where all the four 64-pin connectors are implemented.

Table 2—Pin use comparison, PCI to PMC (single size)

Power pins	Bus pins	PCI	PMC
+ 5 V		8	6
+ 12 V		1	1
- 12 V		1	1
+ 3.3 V		12	9
V (I/O		11	8
Ground		42	43
Subtotal		75	69
	Signals	100	101
	BUSMODE	2	4
	I/O	0	64
	PCI	11	11
	PMC	0	8
	Subtotal	113	187
	Total pins	188	256

5.4 Mapping of PCI reserve pins

In the future, should one or more of the PCI reserved pins become assigned to a new function, the assignment to the PMC connector shall be consistent. Table 3 lists the assignment of these reserved pins to the PMC connector. It will not be necessary to update this standard whenever this occurs.

Assignment of PMC reserved pins will require an update to this standard.

Table 3—PCI-reserved/PMC relationship

PCI-RSVD	PMC signal
9A	Pn2-8
10B	Pn2-9
11A	Pn2-10
14B	Pn1-10
40A	Pn1-41
41A	Pn1-42
63B	Pn3-1
92A	Pn3-59
92B	Pn3-60
93B	Pn3-61
94A	Pn3-64